AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-18. (canceled)

19. (currently amended): An information processing apparatus comprising:

a first computer module which includes a controller and a second computer module which includes another controller, wherein:

said each of said first and second computer modules includes a processor, a first memory, and a second memory;

said processors execute the same instructions substantially simultaneously and are substantially synchronized with each other;

said each first memory is read and written by the processor which is ~~or the~~on the same computer module;

said each second memory is read and written by the processor which is on the same computer module and is written by said processor which is on the other computer module;

wherein data is written to the first memory of the first computer module and the same data is written to at least the second memory of the first computer module; and

wherein, during a normal process, ~~each of said controllers controls so that each of~~ said first processor ~~processors~~ works by means of said first memory which is on the ~~same~~first computer module and said second memory is written by said processor which is on the ~~other~~second computer module, and wherein, during a rejoining process, ~~each of said controllers controls so that each of~~ said first processor ~~processors~~ switches from working by means of said first memory which is on the first computer module ~~works~~ to working by means of said second memory which is on the ~~same~~first computer module.

20. (previously presented): The information processing apparatus as claimed in claim 19, wherein said each controller controls so that during the normal process read access from said processor which is on the same computer module is carried out as against said first memory which is on the same computer module and write access from said processor which is on the same computer module is carried out as against said first and said second memories which are on the same computer module and write access from said processor which is on the other computer module is carried out as against said second memory which is on the same computer module, and each controller controls so that, during the rejoining process, read access from said processor which is on the same computer module is carried out as against said second memory which is on the same computer module and write access from said processor which is on the same computer module is carried out as against said first and said second memory which are on the same computer module and said second memory which is on the other computer module.

21. (previously presented): The information processing apparatus as claimed in claim 20, wherein said each controller copies the contents of said second memory which is on the same computer module to said first memory element which is on the same computer module when no read or write access from said processor which is on the same computer module to said second memory is present during the rejoining process.

22. (previously presented): The information processing apparatus as claimed in claim 21, wherein said each controller copies the contents of said second memory to said first memory by means of a direct memory access circuit.

23. (previously presented): The information processing apparatus as claimed in claim 21, wherein a state of said computer module changes to the normal state from the rejoining state when the copy is completed for all memory areas of said second memory.

24. (previously presented): The information processing apparatus as claimed in claim 22, wherein a state of said computer module changes to a normal state from the rejoining state when the copying is completed for all memory areas of said second memory.

25. (previously presented): The information processing apparatus as claimed in claim 19, wherein said controllers are connected as a ring for three or more said computer modules.

26. (previously presented): The information processing apparatus as claimed in claim 20, wherein said controllers arc connected as a ring for three or more said computer modules.

27. (previously presented): The information processing apparatus as claimed in claim 21, wherein said controllers are connected as a ring for three or more said computer modules.

28. (previously presented): The information processing apparatus as claimed in claim 22, wherein said controllers are connected as a ring for three or more said computer modules.

29. (previously presented): The information processing apparatus as claimed in claim 23, wherein said controllers are connected as a ring for three or more said computer modules.

30. (previously presented): The information processing apparatus as claimed in claim 24, wherein said controllers are connected as a ring for three or more said computer modules.

31. (previously presented): The information processing apparatus as claimed in claim 19, wherein said first and second computer modules are on lockstep fault tolerant computer system.

32. (previously presented): The information processing apparatus as claimed in claim 20, wherein said first and second computer modules are on lockstep fault tolerant computer system.

33. (previously presented): The information processing apparatus as claimed in claim 21, wherein said first and second computer modules are on lockstep fault tolerant computer system.

34. (previously presented): The information processing apparatus as claimed in claim 22, wherein said first and second computer modules are on lockstep fault tolerant computer system.

35. (previously presented): The information processing apparatus as claimed in claim 24, wherein said first and second computer modules are on lockstep fault tolerant computer system.

36. (previously presented): The information processing apparatus as claimed in claim 30, wherein said first and second computer modules are on lockstep fault tolerant computer system.

37. (new): An information processing apparatus comprising:

a computer module comprising a first processor, a first memory and a second memory; and

a second processor apart from said computer module and executing the same instructions substantially simultaneously with said first processor;

wherein said first processor writes data to said first memory and said second processor writes said data to said second memory substantially simultaneously, and said first processor switches from reading said data from said first memory in a first state to reading said data from said second memory in a second state.